WHAT IS CLAIMED IS:

1. A motherboard with reduced power consumption, comprising:

a memory module slot for connecting a memory module;

a DDR (Double data rate) termination array, coupled to the memory module slot for providing a plurality of termination resistors connected between a voltage source and the memory module slot, wherein connections between the voltage source and the termination resistors are controlled according to an indication of a control signal; and

a controller chip set, coupled to the memory module slot and the DDR termination array to provide the control signal, wherein when the motherboard enters a power saving mode, or before the memory module is inserted into the memory module slot, the control signal commands the DDR termination array to cut off the connections between the termination resistors and the voltage source.

2. The motherboard according to claim 1, wherein the control signal includes a clock enable signal.

3. The motherboard according to claim 1, wherein the memory module comprises a double data rate dynamic random access memory (DDR DRAM).

4. The motherboard according to claim 1, wherein the motherboard is used in a laptop computer.

5. The motherboard according to claim 1, wherein the controller chip set comprises a north bridge chip.

6. The motherboard according to claim 1, wherein the DDR termination array comprises:

a plurality of signal terminals, coupled to a plurality of corresponding signal buses;

a plurality of switches, wherein each of the switches comprises a first terminal, a second terminal and a control terminal, and each of the first terminals is connected to one of the signal terminals; and

wherein the control signal commands the switches being switched on or off for controlling the connections between the termination resistors and the voltage source .

7. The motherboard according to claim 1, wherein the DDR termination array comprises:

a plurality of signal terminals, coupled to a plurality of corresponding signal buses;

a switch, comprising a first terminal, a second terminal and a control terminal, the first terminal being connected to the voltage source; and

wherein each one of the termination resistors is connected between one of he signal terminals and the second terminal of the switch, and the control terminal of the switch receives the control signal to turn the switch on or off according to an indication of the control signal.

8. A motherboard with reduced power consumption, comprising:

a memory module slot for connecting a memory module;

a plurality of termination resistors, each of the termination resistors comprises a first terminal and a second terminal, wherein the first terminals of the termination resistors are coupled to the memory module slot;

a switch, comprising a first terminal, a second terminal and a control terminal, wherein the second terminals of the termination resistors are coupled to the first terminal of the switch, the second terminal of the switch is coupled to a voltage source, and the control terminal is used to receive a control signal; and

a controller chip set, coupled to the memory module slot and the switch to provide the control signal, wherein when the motherboard enters a power saving mode or when the memory module is not inserted in the memory module slot, the control signal commands the switch to cut off the connection between the termination resistors and the voltage source.

9. The motherboard according to claim 8, wherein the control signal comprises a clock enable signal.

10. The motherboard according to claim 8, wherein the memory module comprises a double data rate dynamic random access memory (DDR DRAM).

11. The motherboard according to claim 8, wherein the motherboard is used in a laptop computer.

12. The motherboard according to claim 8, wherein the controller chip set comprises a north bridge chip.

13. An operation method of a motherboard with reduced power consumption, wherein the motherboard comprises a memory module slot and a plurality of termination resistors, the termination resistors, the memory module slot and a voltage source form an operation circuit, the operation method comprising:

providing a control signal wherein a connection between the voltage source and the operation circuit is controlled by an indication of the control signal;

using the control signal to cut off the connection between the voltage source and the operation circuit when the motherboard enters a power saving mode or when the memory module slot is not inserted with a memory module; and

using the control signal to establish the connection between the voltage source and the operation circuit when the motherboard enters a normal operation mode and when the

memory module slot is inserted with the memory module.

14. The operation method according to claim 13, wherein the cutting off step comprises a step of cutting off connections between the termination resistors and the memory module slot.

15. The operation method according to claim 13, wherein the cutting off step comprises a step of cutting off connections between the termination resistors and the voltage source.

16. The operation method according to claim 13, wherein the control signal is an clock enable signal provided by a laptop computer.